

	Class	Subclass
ISSUE CLASSIFICATION		

PATENT NUMBER

U.S. **UTILITY** Patent Application

O.I.P.E.

PATENT DATE

SCANNED SBR Q.A. AC

APPLICATION NO. 09/975064	CONT/PRIOR	CLASS 324 714	SUBCLASS 718	ART UNIT 2858 2133	EXAMINER 2858 714
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APPLICANTS

TITLE

Efficient test structure for non-volatile memory and other semiconductor integrated circuits

PTO-2040
12/99

ISSUING CLASSIFICATION												
ORIGINAL				CROSS REFERENCE(S)								
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)							
INTERNATIONAL CLASSIFICATION												

☐ Continued on Issue Slip inside File Jacket.

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS		CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed. <input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____ <input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Assistant Examiner) (Date)		NOTICE OF ALLOWANCE MAILED	
	_____ (Primary Examiner) (Date)		ISSUE FEE	
			Amount Due	Date Paid
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